What is claimed is:

1   1. A method for performing DMA transfers with dynamic
2   descriptor structure, comprising the steps of:
3   creating a new chain of descriptors each including an
4   end-of-chain entry set to a false value except a
5   dummy descriptor at the end of the new chain
6   having the end-of-chain entry set to a true
7   value, wherein each of the descriptors excluding
8   the dummy descriptor further comprises one or
9   more parameters identifying data to be
10   transferred and a link pointer specifying a next
11   descriptor within the new chain;
12   appending the new descriptor chain to a previous
13   descriptor chain, if any, by transferring the
14   parameters and the link pointer of the first
15   descriptor within the new descriptor chain to a
16   dummy descriptor of the previous descriptor
17   chain;
18   changing the end-of-chain entry of the dummy descriptor
19   within the previous descriptor chain from the
20   true value to the false value;
21   fetching the descriptor specified by a next address;
22   determining whether the end-of-chain entry of the
23   currently fetched descriptor is set to the false
24   value;
25   if so, updating the next address with the link pointer
26   of the currently fetched descriptor; and
27   transferring the data identified in the parameter of
28   the currently fetched descriptor.

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1   2. The method as recited in claim 1 further comprising
2   the step of issuing a command after the new descriptor chain
3   is appended to the previous descriptor chain.

1   3. The method as recited in claim 2 further comprising
2   the step of causing the next address to point to the first
3   descriptor within the new descriptor chain before the
4   issuing step.

1   4. The method as recited in claim 2 further comprising
2   the step of ignoring the issued command if the data transfer
3   identified in the previous descriptor chain is being
4   performed.

1   5. The method as recited in claim 2 further comprising
2   the step of accepting the issued command if there are no
3   more data transfers identified in the previous descriptor
4   chain.

1   6. The method as recited in claim 1 wherein the
2   fetching step through the transferring step are executed in
3   a loop until the end-of-chain entry with the true value is
4   detected in the determining step.

1   7. The method as recited in claim 5 wherein, after
2   acceptance of the issued command, the fetching step through
3   the transferring step are executed in a loop until the end-
4   of-chain entry with the true value is detected in the
5   determining step.

1   8. A method for performing DMA transfers under control

2   of a DMA controller and a processor, the method comprising

3   the steps of:

4   creating a chain of descriptors each including an end-

5   of-chain entry set to a false value except a

6   dummy descriptor at the end of the descriptor

7   chain having the end-of-chain entry set to a true

8   value, wherein each of the descriptors excluding

9   the dummy descriptor further comprises one or

10   more parameters identifying data to be

11   transferred by the DMA controller and a link

12   pointer specifying a next descriptor within the

13   descriptor chain;

14   causing a starting address to point to the first

15   descriptor within the descriptor chain;

16   issuing a start command by the processor;

17   accepting the start command by the DMA controller which

18   is in an idle state;

19   replacing a next address with the starting address;

20   from the descriptor chain, fetching the descriptor

21   specified by the next address;

22   determining whether the end-of-chain entry of the

23   currently fetched descriptor is set to the false

24   value;

25   if so, updating the next address with the link pointer

26   of the currently fetched descriptor;

27   transferring the data identified in the parameters of

28   the currently fetched descriptor; and

29   repeating the fetching through the transferring steps

30   until the end-of-chain entry with the true value

31   is detected in the determining step.

1   9. The method as recited in claim 8 further comprising

2 the steps of:

3   creating a new chain of descriptors;

4   appending the newly created descriptor chain to the

5   previously   created   descriptor   chain   by

6   transferring parameters and a link pointer of the

7   first   descriptor   within   the   newly   created

8   descriptor chain to the dummy descriptor of the

9   previously created descriptor chain;

10   changing the end-of-chain entry of the dummy descriptor

11   within   the   previously   created   descriptor   chain

12   from the true value to the false value;

13   issuing a resume command by the processor; and

14   ignoring   the   resume   command   if   the   data   transfer

15   identified   in   the   previously   created   descriptor

16   chain is being performed by the DMA controller.

1   10. The method as recited in claim 9 further comprising

2 the   step   of   accepting   the   resume   command   by   the   DMA

3 controller if there are no more data transfers identified in

4 the previously created descriptor chain.

1   11. The method as recited in claim 10 wherein, after

2 acceptance of the resume command, the fetching through the

3 transferring steps are resumed in a loop until the end-of-

4 chain   entry   with   the   true   value   is   detected   in   the

5 determining step.

1   12. A method for performing DMA transfers under control

2 of a DMA controller and a processor, the method comprising

3 the steps of:

4   creating a chain of descriptors each including an end-

5   of-chain entry set to a false value except the

6   last descriptor within the descriptor chain

7   having the end-of-chain entry set to a true

8   value, wherein each of the descriptors further

9   comprises one or more parameters identifying data

10   to be transferred by the DMA controller and a

11   link pointer specifying a next descriptor within

12   the descriptor chain;

13   causing a next address to point to the first descriptor

14   within the descriptor chain;

15   issuing a command by the processor;

16   accepting the issued command by the DMA controller

17   which is in an idle state;

18   from the descriptor chain, reading the descriptor

19   specified by the next address;

20   transferring the data identified in the parameters of

21   the currently read descriptor;

22   determining whether the end-of-chain entry of the

23   currently read descriptor is set to the false

24   value;

25   if so, updating the next address with the link pointer

26   of the currently read descriptor; and

27   repeating the reading through the updating steps until

28   the end-of-chain entry with the true value is

29   detected in the determining step.

1   13.   The   method   as   recited   in   claim   12   further

2   comprising the steps of:

3   creating a new chain of descriptors;

4   appending the newly created descriptor chain to the

5   previously created descriptor chain by causing

6   the link pointer of the last descriptor within

7   the previously created descriptor chain to point

8   to the first descriptor within the newly created

9   descriptor chain;

10   changing the end-of-chain entry of the last descriptor

11   within the previously created descriptor chain

12   from the true value to the false value;

13   issuing the command by the processor; and

14   ignoring the issued command if the data transfer

15   identified in the previously created descriptor

16   chain is being performed by the DMA controller.

1   14.   The   method   as   recited   in   claim   13   further

2   comprising the steps of:

3   if there are no more data transfers identified in the

4   previously created descriptor chain:

5   accepting   the   issued   command   by   the   DMA

6   controller;

7   fetching   the   descriptor   specified   by   the   next

8   address; and

9   replacing the next address with the link pointer

10   of the currently fetched descriptor.

1   15. The method as recited in claim 14 wherein, once the

2   issued   command   is   accepted   by   the   DMA   controller,   the

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3 reading step through the updating step are executed in a

4 loop until the end-of-chain entry with the true value is

5 detected in the determining step.